FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **RCA 89413**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): **10/031090**

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US00/19257	**14 July 2000 (14.07.00)**	**16 July 1999 (16.07.99)**

TITLE OF INVENTION

SPURIOUS FREQUENCIES ATTENUATION FOR A DC REFERENCE VOLTAGE

APPLICANT(S) FOR DO/EO/US

Gerald Adolph Colman and Roderick Andre Watts

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include itens (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☐ has been communicated by the International Bureau.
   c. ☒ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☐ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☒ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

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EXPRESS MAIL LABEL NO. EL902321719US **DATE DEPOSITED: January 15, 2002**

JC13 Rec'd PCT/PTO 15 JAN 2002

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/031090	PCT/US00/19257	RCA 89413

24. The following fees are submitted:.	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :		
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO **$1040.00**		
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO **$890.00**		
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO **$740.00**		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) **$710.00**		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) **$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =	**$890.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS	PTO USE ONLY
Total claims	16 - 20 =	0	x $18.00	**$0.00**	
Independent claims	3 - 3 =	0	x $84.00	**$0.00**	
Multiple Dependent Claims **(check if applicable).**			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$890.00**	
☐ Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**	
SUBTOTAL =				**$890.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$890.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$40.00**	
TOTAL FEES ENCLOSED =				**$930.00**	
				Amount to be: refunded	$
				charged	$ 930.00

a. ☐ A check in the amount of ________ to cover the above fees is enclosed.

b. ☒ Please charge my Deposit Account No. **07-0832** in the amount of **$930.00** to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **07-0832** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Mr. Joseph S. Tripoli
THOMSON multimedia Licensing Inc.
Patent Department
PO Box 5312
Princeton, New Jersey 08540

[signature]
SIGNATURE

ROBERT D. SHEDD
NAME

36,269
REGISTRATION NUMBER

January 15, 2002
DATE

EXPRESS MAIL LABEL NO. EL902321719US RCA 89413

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Gerald Adolph Colman and Roderick Andre Watts

Filed : Herewith

For : SPURIOUS FREQUENCIES ATTENUATION FOR A DC REFERENCE VOLTAGE

PRELIMINARY AMENDMENT

Hon. Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Sir:

In the US national phase application of PCT/US00/19257 filed herewith, please enter the following amendments:

IN THE SPECIFICATION:

Please amend the specification as follows: A marked up version of the amended specification is attached herewith:

On Page 1, please amend the first paragraph as follows:

--This application claims the benefit under 35 U.S.C. § 365 of International Application PCT/US00//19257, filed July 14, 2000, which was published in accordance with PCT Article 21(2) on January 25, 2001 in English; and which claims benefit of U.S. Provisional Patent Application Serial No. 60/144,426 filed on July 16, 1999.--

IN THE CLAIMS:

Please amend the claims (which are the annexes of the International Preliminary Examination Report) as follows. A marked-up version of the claims is attached herewith:

1.(AMENDED) A television apparatus comprising a processing circuitry adapted to receive an analog television signal, comprising:

a video decoder coupled to the processing circuitry and adapted to process the analog television signal, the video decoder adapted to provide luminance signal restoration and configured with a luminance voltage offset reference terminal adapted to aid in the luminance signal restoration; and

a circuit for luminance signal restoration in an analog television signal video decoder which is coupled to the luminance voltage offset terminal.

2.(AMENDED) The television apparatus of claim 1, further comprising the luminance signal restoration circuit comprises a first, second and third branch, parallel circuit.

3.(AMENDED) The television apparatus of claim 2, further comprising the first branch includes a first capacitor coupled between an analog ground and the luminance voltage offset terminal, the second branch includes a first resistor coupled in series in with a second capacitor, the first resistor and second capacitor coupled between the analog ground and the luminance voltage offset terminal, and the third branch includes third capacitor coupled between the analog ground and the luminance voltage offset terminal.

4.(AMENDED) The television apparatus of claim 3, further comprising the first capacitor has a value of approximately 820 pF, the second capacitor has a value of approximately 6.8uF, the third capacitor has a value of approximately 0.27uF, and the first resistor has a value of approximately 720 Ohms.

5.(AMENDED) The television apparatus of claim 3, further comprising the first resistor of the second branch is coupled to the luminance voltage offset terminal, and the second capacitor is coupled to the analog ground [(64)].

6.(AMENDED) The television apparatus of claim 3, further comprising values for each component of the first, second and third branches are selected to filter a particular frequency.

7.(AMENDED) In a television apparatus adapted to receive analog television signals, and having processing circuitry and a video decoder for the analog television signals, wherein:

a video decoder having a luminance restoration terminal in communication with luminance restoration circuitry, and a circuit for luminance signal restoration circuitry comprising:

a first circuit branch;

a second circuit branch;

a third circuit branch; and

wherein said first, second, and third branches are in parallel.

8.(AMENDED) The luminance signal restoration circuit of claim 7, further comprising said first circuit branch include a first capacitor, said second circuit branch includes a first resistor in series with a second capacitor and said third circuit branch includes a third capacitor.

9.(AMENDED) The luminance signal restoration circuit of claim 8, further comprising said first capacitor is coupled between the luminance restoration terminal and an analog ground, said first resistor is coupled

between the luminance restoration terminal and said second capacitor which is coupled between said first resistor and the analog ground, and said third capacitor is coupled between the luminance restoration terminal and the analog ground.

10.(AMENDED) The luminance signal restoration circuit of claim 9, further comprising said first capacitor has a value of approximately 820 pF, said second capacitor has a value of approximately 6.8 uF, said third capacitor has a value of approximately 0.27 uF, and said first resistor has a value of approximately 720Q Ohms.

11.(AMENDED) The luminance signal restoration of claim 9, further comprising values for each component of said first, second, and third branches are selected to filter a particular frequency.

12.(AMENDED) In a television apparatus adapted to receive analog television signals, the television apparatus having a signal decoding integrated circuit wherein:

the signal decoding integrated circuit having luminance signal restoration capabilities and a luminance voltage offset terminal, and a luminance signal restoration circuit comprising:

a first circuit branch configured to attenuate a first frequency;

a second circuit branch configured to attenuate a second frequency; and

a third circuit branch configured to attenuate a third frequency.

13.(AMENDED) The luminance signal restoration circuit of claim 12, further comprising said first, second and third circuit branches are in parallel.

14.(AMENDED) The luminance signal restoration circuit of claim 13, further comprising said first circuit branch includes a first capacitor, said second circuit branch includes a first resistor in series with a second capacitor, and said third circuit branch includes a third capacitor.

15.(AMENDED) The luminance signal restoration circuit of claim 14, further comprising said first capacitor is coupled between the luminance voltage offset terminal and an analog ground, said first resistor is coupled between the luminance voltage offset terminal and said second capacitor which is coupled between said first resistor and the analog ground, and said third capacitor is coupled between the luminance voltage offset terminal and the analog ground.

16.(AMENDED) The luminance signal restoration circuit of claim 15, further comprising said first capacitor has a value of approximately 820 pF, said second capacitor has a value of approximately 6.8uF, said third capacitor has a value of approximately 0.27uF, and said first resistor has a value of approximately 720 Ohms.

IN THE ABSTRACT:

Please add the following Abstract.

-- In a television apparatus that includes a television signal decoding integrated circuit that performs combing, PIP, OSD, chroma and luminance decoding, digitizing, and other functions, particularly on analog signals, an automatic gain control circuit is coupled to the television signal decoding IC at its luminance DC restoration pinout. The AGC circuit provides an improved NTSC signal picture by filtering out unwanted noise and oscillations. --

REMARKS

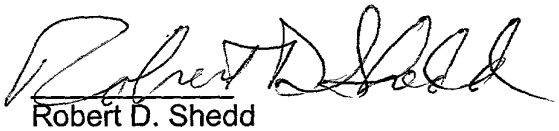
The specification has been amended to include a reference to the priority applications.

The claims have been amended to remove reference indicia and to meet the requirements of the United States.

To meet the requirements of the United States, the Abstract (as originally filed in the PCT application) is added.

No fee is believed to have been incurred by virtue of this amendment. However if a fee is incurred on the basis of this amendment, please charge such fee against deposit account 07-0832

Respectfully submitted,
Gerald Adolph Colman
Roderick Andre Watts



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January 15, 2002

MARKED UP VERSION OF THE AMENDED SPECIFICATION

On Page 1, please amend the first paragraph as follows:

--This application claims the benefit under 35 U.S.C. § 365 of International Application PCT/US00//19257, filed July 14, 2000, which was published in accordance with PCT Article 21(2) on January 25, 2001 in English; and which claims benefit of U.S. Provisional Patent Application Serial No. 60/144,426 filed on July 16, 1999.--

MARKED-UP VERSION OF THE AMENDED CLAIMS

Please amend the claims (which are the annexes of the International Preliminary Examination Report) as follows. A marked-up version of the claims is attached herewith:

1.(AMENDED) A television apparatus [(12)] comprising a processing circuitry adapted to receive an analog television signal, [characterized by] comprising:

a video decoder [(50)] coupled to the processing circuitry and adapted to process the analog television signal, the video decoder adapted to provide luminance signal restoration and configured with a luminance voltage offset reference terminal [(76)] adapted to aid in the luminance signal restoration; and

a circuit for luminance signal restoration [(60)] in an analog television signal video decoder which is coupled to the luminance voltage offset terminal [(76)].

2.(AMENDED) The television apparatus [(12)] of claim 1, further [characterized in that] comprising the luminance signal restoration circuit [(60)] comprises a first [(70)], second [(80)] and third [(90)] branch, parallel circuit.

3.(AMENDED) The television apparatus [(12)] of claim 2, further [characterized in that] comprising the first branch [(70)] includes a first capacitor [(C2)] coupled between an analog ground [(64)] and the luminance voltage offset terminal [(76)], the second branch [(80)] includes a first resistor [(R1)] coupled in series in with a second capacitor [(C2)], the first resistor [(R1)] and second capacitor [(C2)] coupled between the analog ground [(64)] and the luminance voltage offset terminal [(76)], and the third branch [(90)]

includes third capacitor [(C3)] coupled between the analog ground [(64)] and the luminance voltage offset terminal [(76)].

4.(AMENDED) The television apparatus [(12)] of claim 3, further [characterized in that] comprising the first capacitor [(C1)] has a value of approximately 820 pF, the second capacitor [(C2)] has a value of approximately 6.8uF, the third capacitor [(C3)] has a value of approximately 0.27uF, and the first resistor [(R1)] has a value of approximately 720 Ohms.

5.(AMENDED) The television apparatus [(12)] of claim 3, further [characterized in that] comprising the first resistor [(R1)] of the second branch [(80)] is coupled to the luminance voltage offset terminal [(76)], and the second capacitor [(C2)] is coupled to the analog ground [(64)].

6.(AMENDED) The television apparatus [(12)] of claim 3, further [characterized in that] comprising values for each component of the first [(70)], second [(80)] and third [(90)] branches are selected to filter a particular frequency.

7.(AMENDED) In a television apparatus [(12)] adapted to receive analog television signals, and having processing circuitry and a video decoder [(50)] for the analog television signals, [characterized by] wherein:

a video decoder [(50)] having a luminance restoration terminal [(76)] in communication with luminance restoration circuitry [(60)], and a circuit [(60)] for luminance signal restoration circuitry comprising:

a first circuit branch [(70)];

a second circuit branch [(80)];

a third circuit branch [(90)]; and

wherein said first [(70)], second [(80)], and third [(90)] branches are in parallel.

8.(AMENDED) The luminance signal restoration circuit [(60)] of claim 7, further [characterized in that] comprising said first circuit branch [(70)] include a first capacitor [(C1)], said second circuit branch [(80)] includes a first resistor [(R1)] in series with a second capacitor [(C2)], and said third circuit branch [(90)] includes a third capacitor [(C3)].

9.(AMENDED) The luminance signal restoration circuit [(60)] of claim 8, further [characterized in that] comprising said first capacitor [(C1)] is coupled between the luminance restoration terminal [(76)] and an analog ground [(64)], said first resistor [(R1)] is coupled between the luminance restoration terminal [(76)] and said second capacitor [(C2)] which is coupled between said first resistor [(R1)] and the analog ground [(64)], and said third capacitor [(C3)] is coupled between the luminance restoration terminal [(76)] and the analog ground [(64)].

10.(AMENDED) The luminance signal restoration circuit [(60)] of claim 9, further [characterized in that] comprising said first capacitor [(C1)] has a value of approximately 820 pF, said second capacitor [(C2)] has a value of approximately 6.8 uF, said third capacitor [(C3)] has a value of approximately 0.27 uF, and said first resistor [(R1)] has a value of approximately 720Q Ohms.

11.(AMENDED) The luminance signal restoration [(60)] of claim 9, further [characterized in that] comprising values for each component of said first [(70)], second [(80)], and third [(90)] branches are selected to filter a particular frequency.

12.(AMENDED) In a television apparatus [(12)] adapted to receive analog television signals, the television apparatus [(12)] having a signal decoding integrated circuit [(IC) characterized by] wherein:

the signal decoding integrated circuit [(IC)] having luminance signal[)] restoration capabilities and a luminance voltage offset terminal [(76)], and a luminance signal restoration circuit [(6C)] comprising:

a first circuit branch [(70)] configured to attenuate a first frequency;

a second circuit branch [(80)] configured to attenuate a second frequency; and

a third circuit branch [(90)] configured to attenuate a third frequency.

13.(AMENDED) The luminance signal restoration circuit [(60)] of claim 12, further [characterized in that] comprising said first [(70)], second [(80)] and third [(90)] circuit branches are in parallel.

14.(AMENDED) The luminance signal restoration circuit [(60)] of claim 13, further [characterized in that] comprising said first circuit branch [(70)] includes a first capacitor [(C1)], said second circuit branch [(80)] includes a first resistor [(R1)] in series with a second capacitor [(C2)], and said third circuit branch [(90)] includes a third capacitor [(C3)].

15.(AMENDED) The luminance signal restoration circuit [(60)] of claim 14, further [characterized in that] comprising said first capacitor [(C1)] is coupled between the luminance voltage offset terminal [(76)] and an analog ground [(64)], said first resistor [(R1)] is coupled between the luminance voltage offset terminal [(76)] and said second capacitor [(C2)] which is

coupled between said first resistor [(R1)] and the analog ground [(64)], and said third capacitor [(C3)] is coupled between the luminance voltage offset terminal [(76)] and the analog ground [(64)].

16.(AMENDED) The luminance signal restoration circuit [(60] of claim 15, further [characterized in that] comprising said first capacitor [(C1)] has a value of approximately 820 pF, said second capacitor [(C2)] has a value of approximately 6.8uF, said third capacitor [(C3)] has a value of approximately 0.27uF, and said first resistor [(R1)] has a value of approximately 720 Ohms.

SPURIOUS FREQUENCIES ATTENUATION FOR A DC REFERENCE VOLTAGE

This application claims the benefit of U.S. Provisional Patent Application Serial No. 60/144,426 filed on July 16, 1999.

Field of the Invention

The present invention relates to decoders in televisions for decoding received analog audio and video signals or transmissions and, more particularly, to an automatic gain control circuit for a decoder in a television for decoding received analog audio and video signals or transmissions.

Background of the Invention

Televisions and other similar devices must now be able to receive, decode, and process analog and digital audio and video signals or transmissions. Because of the complexity of modern televisions caused by digital television signals and related processing, and analog television signal processing, many of the capabilities and functions thereof are performed by specialized digital integrated circuits (ICs). Advantageously, it is also preferable to manipulate/process the television signal in the digital domain regardless of whether the original received television signal is analog or digital.

Of the various types of ICs used in televisions, decoders and digitizers aid in the processing of the digital and analog television signals. One type of IC that is used in televisions for processing analog television signals is a video decoder. After processing of the analog television signal the video decoder IC generally digitizes the component signals for further processing. However, during processing of the analog signal, it is necessary to provide luminance signal DC restoration.

As an example, the HMP8117 Video Decoder, from Intersil Corporation, is one type of video decoder that accepts incoming analog NTSC or PAL television signals, processes the analog television signal, digitizes the signals, and then processes/manipulates the digital signals. The HMP 8117 is particularly designed

to decode baseband composite or S-video NTSC and PAL signals. Other functions are also supported.

In the HMP8117 video decoder, analog signal processing includes the restoration of a luminance signal (luminance signal restoration). Luminance signal restoration is a necessary step of television signal processing. In the HMP8117, a luminance control terminal or pin (LCAP) is furnished to provide a voltage to offset the sync tip of the luminance circuitry to a lower reference of an internal A/D converter. It is recommended by the manufacturer of the HMP8117 to couple a single storage capacitor of a given value to the LCAP pin. Such is typical of video decoders for analog signals.

It has been determined, however, that a single storage capacitor for the luminance circuitry does not provide a quality picture when the incoming, original television signal is analog. This is due to noise and oscillations that appear in the luminance decoding because of the analog signal.

Summary of the Invention

The present invention comprises an automatic gain control network or circuit for luminance signal restoration in an analog television signal video decoder. The video decoder is preferably an integrated circuit (IC) that receives the analog video television signal or transmission.

In one form, the present invention comprises a television apparatus that includes processing circuitry adapted to receive an analog television signal, a video decoder coupled to the processing circuitry and adapted to process the analog television signal, the video decoder adapted to provide luminance signal restoration and configured with a luminance voltage offset reference terminal adapted to aid in the luminance signal restoration, and an automatic gain control network coupled to the luminance voltage offset terminal.

In another form, the present invention comprises an automatic gain control network for luminance restoration circuitry in a television apparatus, wherein the television is adapted to receive analog television signals, and includes processing circuitry and a video decoder for the analog television signals, the video decoder having a luminance restoration terminal in communication with the luminance

restoration circuitry. The automatic gain control network for the luminance restoration circuitry includes, a first circuit branch, a second circuit branch, and a third circuit branch. The first, second, and third branches being situated in parallel.

In still another form, the present invention comprises an automatic gain control network for a television apparatus, wherein the television apparatus is adapted to receive analog television signals, has a signal decoding integrated circuit, with the signal decoding integrated circuit having luminance signal restoration capabilities and a luminance voltage offset terminal. The automatic gain control network includes a first circuit branch configured to attenuate a first frequency, a second circuit branch configured to attenuate a second frequency, and a third circuit branch configured to attenuate a third frequency.

Brief Description of the Drawings

Reference to the following description of the present invention should be taken in conjunction with the accompanying drawings, wherein:

Fig. 1 is a block diagram of an exemplary system in which the present invention is utilized;

Fig. 2 is a diagram of an exemplary television apparatus circuit as used in the system of Fig. 1 incorporating the principles of the present invention; and

Fig. 3 is a diagram of an exemplary automatic gain control circuit as used in the television apparatus circuit of Fig. 2.

Corresponding reference characters indicate corresponding parts throughout the several views.

Detailed Description of the Invention

With reference to Fig. 1, there is shown a block diagram of a system, generally designated 10, which may utilize the present invention. It should be initially appreciated that the system 10 depicted in Fig. 1 is only exemplary and/or representational of the many systems that may utilize the principles of the present invention.

The system 10 includes a television apparatus that may or may not include a monitor or other similar display device (collectively "television apparatus") generally designated 12. The television apparatus 12 is adapted through appropriate circuitry, software, and/or other components to decode and process digitally modulated analog audio and video television signals or transmissions ("digital television signals") from a Direct Broadcast Satellite (DBS) system 18 as received via a link or line 20. Such signals may be digitally modulated using the QPSK (Quadrature Phase Shift Keying) format. The television apparatus 12 is also adapted through appropriate circuitry, software, and/or other components to decode and process digital television signals from terrestrial Digital Television (DTV) antenna 14 as received via a link or line 16, such as ATSC DTV. Such signals may be digitally modulated using VSB (Vestigal SideBand).

The television apparatus 12 is also adapted through appropriate circuitry, software, and/or other components, to process analog audio and video television signals ("analog television signals") from a terrestrial analog antenna 22 as received via a link or line 24, as well as analog television signals from a CATV system 26 via a link or line 28. Such processing typically includes digitizing the video and/or audio signals through appropriate circuitry, software, and/or other components. Digital television signals from the CATV system 26 are also decoded and processed as indicated above. It should be appreciated that the television apparatus 12 is adapted to receive and process analog and/or digital television signals from sources other than that shown.

As an example of the above, the television apparatus 12 may be a model DTC 100, from Thomson Consumer Electronics, Inc. of Indianapolis, Indiana. In any form, the television apparatus 12 typically includes appropriate circuitry, software, and other components to support/provide a display, an integral control system, a user-interface and on-screen display (OSD) functionality. It should be appreciated that the television apparatus 12 may take other forms and have additional capabilities and/or functionality other than those shown and/or discussed through appropriate circuitry, software, and/or other components.

Referring to Fig. 2, there is shown a block diagram of at least some of the various components of the DTC 100 television apparatus 12. The DTC 100 television apparatus 12 is adapted through appropriate circuitry, software, and/or other components, to receive and process digital television signals and analog television signals. The various blocks and interconnections depicted in Fig. 2 are exemplary of a television capable utilizing analog and digital television signals. Thus, variations in the interconnections and components may vary.

The television apparatus 12 includes a DSS tuner/IF converter 30 that is adapted to receive a digital television signal (audio, video, and VBI/other) via line 20, allows tuning to the various channels of the digital television signal, converts the digital television signal into an Intermediate Frequency (IF), and sends the IF digital television signal (here shown as QPSK modulated) to a DSS link 32. The DSS link 32 demodulates the IF digital television signal and forwards the resulting digital television signal to a link multiplexer (MUX) 34. The link MUX 34 selectively sends the digital television signal to an ARM transport 36. The ARM transport 36 extracts a digital audio signal that is sent to an MPEG/AC-3 audio decoder 38. The audio decoder 38 decodes the digital audio signal, and sends the decoded digital audio signal to a digital to analog (D/A) converter 44. The D/A converter 44 sends the resulting analog audio signal to an audio processor 46 which send the process analog audio signal to audio amps 48 that are connected to audio speakers.

The ARM transport 36 also extracts a digital video signal that is sent to the decoder 50. The decoder 50 provides necessary MPEG circuitry and/or software to decode the digital video signal. The decoded digital video signal is sent to a digital to analog (D/A) converter and filter 52 to provide an analog television signal for further processing before being forwarded to the display.

The television apparatus 12 also includes a High Definition (HD)/NTSC tuner/IF converter and splitter 40 that receives an HD digital television signal (audio, video, and VBI/other) from the terrestrial digital antenna 14 via line 16, allows tuning to the various channels of the HD digital television signal, converts the HD digital television signal into an Intermediate Frequency (IF), and sends the HD IF digital television signal (here shown as VSB modulated) to an HDTV link

42. The HDTV link 42 demodulates the HD IF digital television signal and forwards the resulting digital signal to a link multiplexer (MUX) 34. The link MUX 34 selectively sends the digital signal to an ARM transport 36. The ARM transport 36 extracts a digital audio signal that is sent to an MPEG/AC-3 audio decoder 38. The audio decoder 38 decodes the digital audio signal, and sends the decoded digital audio signal to a digital to analog (D/A) converter 44. The D/A converter 44 sends the resulting analog audio signal to an audio processor 46 which send the process analog audio signal to audio amps 48 that are connected to audio speakers.

The ARM transport 36 also extracts a digital video signal that is sent to the decoder 50. The decoder 50 provides necessary MPEG circuitry and/or software to decode the digital video signal. The decoded digital video signal is sent to a digital to analog (D/A) converter and filter 52 to provide an analog television signal for further processing before being forwarded to the display.

The High Definition (HD)/NTSC tuner/IF converter and splitter 40 also receives digital television signals from the digital cable source 26 via line 28 and processes them in the same manner as for the terrestrial digital television signals. Additionally, the High Definition (HD)/NTSC tuner/IF converter and splitter 40 provides PIP (Picture-In-Picture) capabilities.

The High Definition (HD)/NTSC tuner/IF converter and splitter 40 also receives analog (NTSC) television signals from the terrestrial analog antenna 22 via line 24 and from the analog cable source 26 via line 28. The analog television signal is tuned by the tuner to a channel of the television signal and provides an IF analog television signal to an NTSC video switcher 56. The NTSC video switcher 56 provides the analog television signal to an initial comb filter/PIP and Chroma decoder 58 after which the analog television signal is sent to an NTSC YUV A/D converter 66 before being sent to the decoder 50.

The television signal decoding integrated circuit (IC) or chip 50 performs combing, picture-in-picture (PIP), chroma decoding and digitizing, MPEG video decoding, NTSC and PAL video upconversion, OSD, and other functions. Such a decoding IC may be an HMP8117 Video Decoder from Intersil Corporation of Palm Bay, Florida (formally Harris Semiconductor of Harris Corporation of

Melbourne Florida), the Harris Semiconductor Data Sheet of January 1999, File Number 4643, of which is specifically incorporated herein by reference.

With additional reference to Fig. 3, the decoding IC 50 is shown in a simplified block form. The decoding IC 50 also performs luminance signal DC restoration for the incoming analog television signal. In particular, the data sheet for the decoding IC 50 indicates that a storage capacitor should be attached to the LCAP (Luminance CAPacitor) pin 76 for providing luminance signal DC restoration. The value of the capacitor is stated to be 0.1μF, and should be connected between the LCAP pin 76 and an AGND (Analog GrouND) pin (not shown).

In accordance with the principles of the present invention, instead of the single storage capacitor being connected to the LCAP pin 76 as suggested by the manufacturer, an automatic gain control (AGC) network or circuit 60 is connected to the LCAP pin 76 and ground. The LCAP voltage offsets a sync tip to the lower reference of an A/D converter (not shown) of the decoder 50. The AGC network 60 improves the quality of the resulting picture of the television apparatus 12 over a single storage capacitor by filtering out unwanted noise and oscillations.

The AGC network 60 is a branched, parallel network having a node 62 and a common ground 64. A first leg or branch 70, situated between the node 62 and the ground 64, includes a capacitor C1 for filtering out first frequencies of noise and/or oscillations. The capacitor C1 may have a value of 820pF. A second leg or branch 80, situated between the node 62 and the ground 64 and parallel to the first leg 70, includes a resistor R1 in series with a capacitor C2. The second leg 70 filters out second frequencies of noise and/or oscillations. The resistor R1 may have a value of 750Ω, while the capacitor C2 may have a value of 6.8μF. The AGC 60 includes a third leg or branch 90 situated between the node 62 and the ground 64 and parallel to the first and second legs 70 and 80. The third leg 90 filters out third frequencies of noise and/or oscillations, and may have a value of 0.27μF.

It should be appreciated that capacitor and resistor values may deviate from those stated above, depending on the desired filtering characteristics of the

AGC network 60. As well, networks other than the branched network 60 shown in Fig. 3 may be used.

While this invention has been described as having a preferred design and/or configuration, the present invention can be further modified within the spirit and scope of this disclosure. This application is therefore intended to cover any variations, uses, or adaptations of the invention using its general principles. Further, this application is intended to cover such departures from the present disclosure as come within known or customary practice in the art to which this invention pertains and which fall within the limits of the appended claims.

1. A television apparatus (12) comprising a processing circuitry adapted to receive an analog television signal, characterized by:

a video decoder (50) coupled to the processing circuitry and adapted to process the analog television signal, the video decoder adapted to provide luminance signal restoration and configured with a luminance voltage offset reference terminal (76) adapted to aid in the luminance signal restoration; and

a circuit for luminance signal restoration (60) in an analog television signal video decoder which is coupled to the luminance voltage offset terminal (76).

2. The television apparatus (12) of claim 1, further characterized in that the luminance signal restoration circuit (60) comprises a first (70), second (80) and third (90) branch, parallel circuit.

3. The television apparatus (12) of claim 2, further characterized in that the first branch (70) includes a first capacitor C2) coupled between an analog ground (64) and the luminance voltage offset terminal (76), the second branch (80) includes a first resistor (R1) coupled in series in with a second capacitor (C2), the first resistor (R1) and second capacitor (C2) coupled between the analog ground (64) and the luminance voltage offset terminal (76), and the third branch (90) includes third capacitor (C3) coupled between the analog ground (64) and the luminance voltage offset terminal (76).

4. The television apparatus (12) of claim 3, further characterized in that the first capacitor (C1) has a value of approximately 820 pF, the second capacitor (C2) has a value of approximately 6.8uF, the third capacitor (C3) has a value of approximately 0.27uF, and the first resistor (R1) has a value of approximately 720 Ohms.

5. The television apparatus (12) of claim 3, further characterized in that the first resistor (R1) of the second branch (80) is coupled to the luminance voltage offset terminal (76), and the second capacitor (C2) is coupled to the analog ground (64).

6. The television apparatus (12) of claim 3, further characterized in that values for each component of the first (70), second (80) and third (90) branches are selected to filter a particular frequency.

7. In a television apparatus (12) adapted to receive analog television signals, and having processing circuitry and a video decoder (50) for the analog television signals, characterized by:

a video decoder (50) having a luminance restoration terminal (76) in communication with luminance restoration circuitry (60), and a circuit (60) for luminance signal restoration circuitry comprising:

a first circuit branch (70);

a second circuit branch (80);

a third circuit branch (90); and

wherein said first (70), second (80), and third (90) branches are in parallel.

8. The luminance signal restoration circuit (60) of claim 7, further characterized in that said first circuit branch (70) include a first capacitor (C1), said second circuit branch (80) includes a first resistor (R1) in series with a second capacitor (C2), and said third circuit branch (90) includes a third capacitor (C3).

9. The luminance signal restoration circuit (60) of claim 8, further characterized in that said first capacitor (C1) is coupled between the luminance restoration terminal (76) and an analog ground (64), said first resistor (R1) is coupled between the luminance restoration terminal (76) and said second capacitor (C2) which is coupled between said first resistor (R1) and the analog ground (64), and said third capacitor (C3) is coupled between the luminance restoration terminal (76) and the analog ground (64).

10. The luminance signal restoration circuit (60) of claim 9, further characterized in that said first capacitor (C1) has a value of approximately 820 pF, said second capacitor (C2) has a value of approximately 6.8 uF, said third capacitor (C3) has a value of approximately 0.27 uF, and said first resistor (R1) has a value of approximately 720Q Ohms.

11. The luminance signal restoration (60) of claim 9, further characterized in that values for each component of said first (70), second (80), and third (90) branches are selected to filter a particular frequency.

12. In a television apparatus (12) adapted to receive analog television signals, the television apparatus (12) having a signal decoding integrated circuit (IC) characterized by:

the signal decoding integrated circuit (IC) having luminance signal) restoration capabilities and a luminance voltage offset terminal (76), and a luminance signal restoration circuit (6C) comprising:

a first circuit branch (70) configured to attenuate a first frequency;

a second circuit branch (80) configured to attenuate a second frequency; and

a third circuit branch (90) configured to attenuate a third frequency.

13. The luminance signal restoration circuit (60) of claim 12, further characterized in that said first (70), second (80) and third (90) circuit branches are in parallel.

14. The luminance signal restoration circuit (60) of claim 13, further characterized in that said first circuit branch (70) includes a first capacitor (C1), said second circuit branch (80) includes a first resistor (R1) in series with a second capacitor (C2), and said third circuit branch (90) includes a third capacitor (C3).

15. The luminance signal restoration circuit (60) of claim 14, further characterized in that said first capacitor (C1) is coupled between the luminance voltage offset terminal (76) and an analog ground (64), said first resistor (R1) is coupled between the luminance voltage offset terminal (76) and said second capacitor (C2) which is coupled between said first resistor (R1) and the analog ground (64), and said third capacitor (C3) is coupled between the luminance voltage offset terminal (76) and the analog ground (64).

16. The luminance signal restoration circuit (60of claim 15, further characterized in that said first capacitor (C1) has a value of approximately 820 pF, said second capacitor (C2) has a value of approximately 6.8uF, said third capacitor (C3) has a value of approximately 0.27uF, and said first resistor (R1) has a value of approximately 720 Ohms.

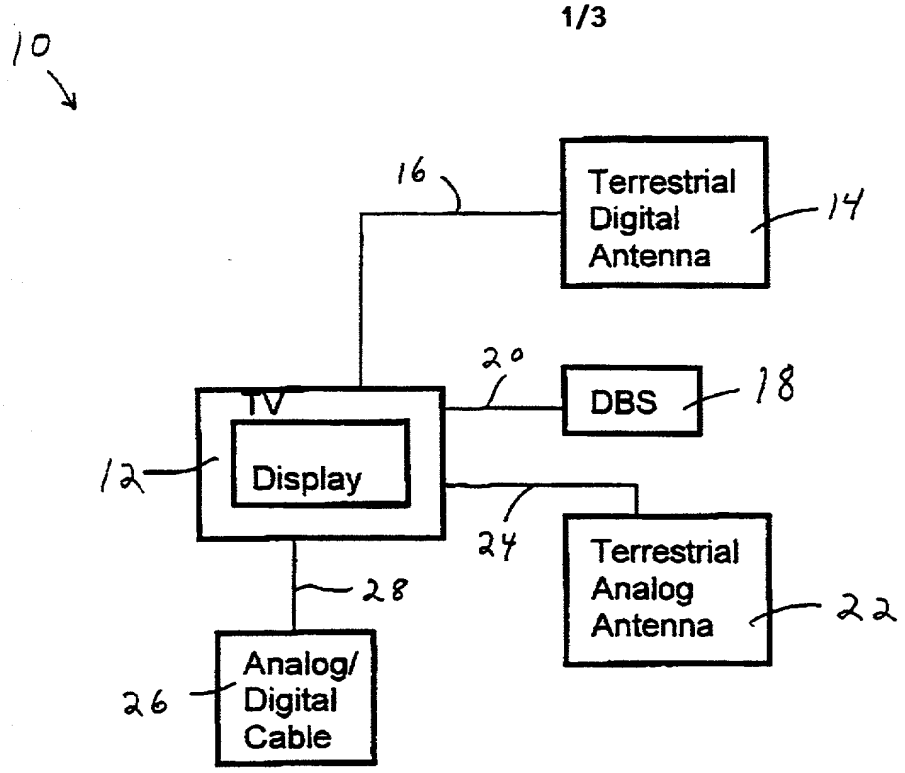

Fig. 1

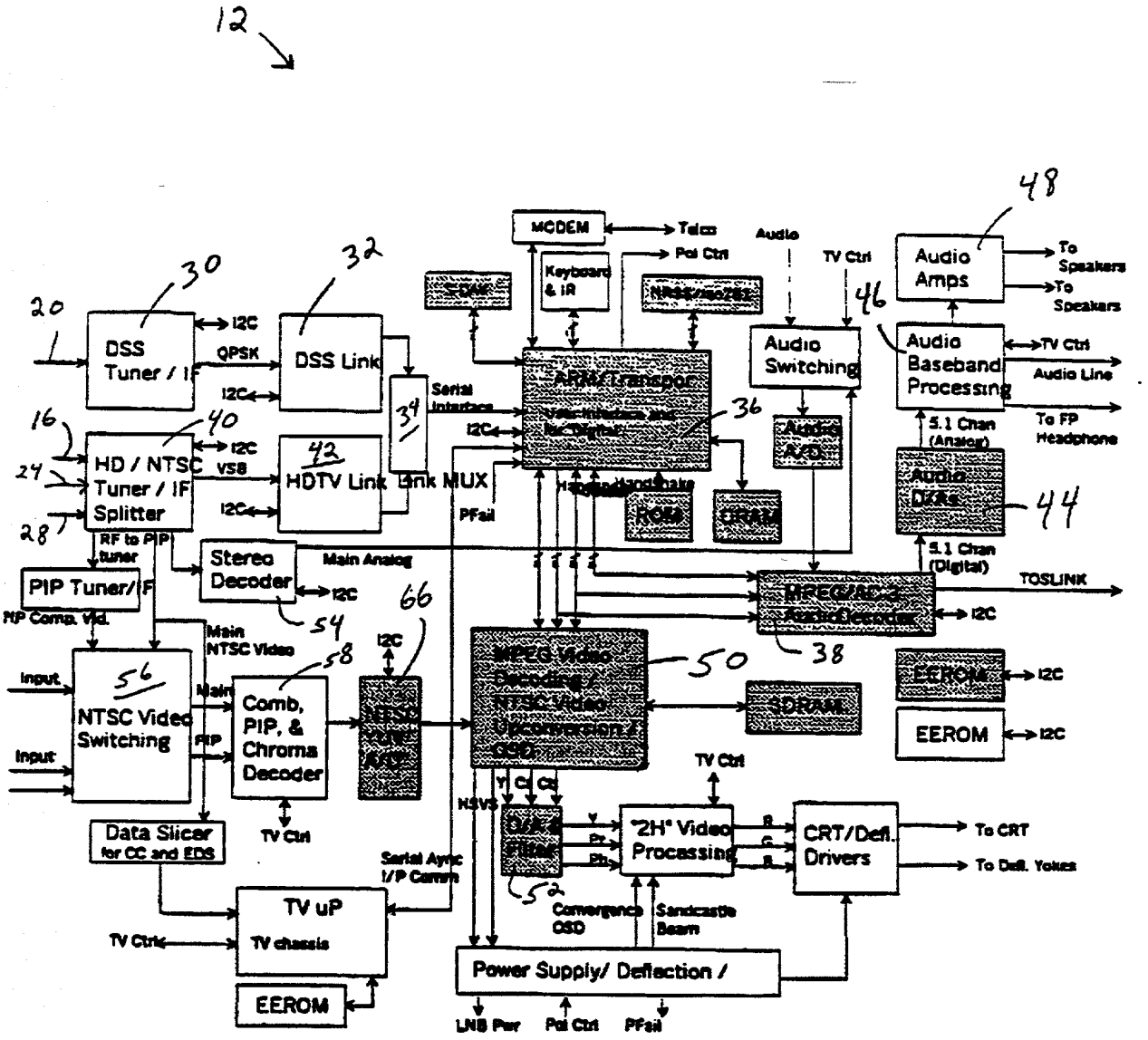
12
20
30
32
48
DSS Tuner / IF
I2C
QPSK
DSS Link
Serial Interface
34
MODEM
Telco
Pol Ctrl
Audio
TV Ctrl
Keyboard & IR
Audio Amps
To Speakers
To Speakers
Audio Switching
46
Audio Baseband Processing
TV Ctrl
Audio Line
To FP Headphone
5.1 Chan (Analog)
Audio D/As
44
5.1 Chan (Digital)
TOSLINK
16
24
28
40
42
HD / NTSC Tuner / IF Splitter
VSB
HDTV Link
Link MUX
PFail
36
ROM
DRAM
RF to PIP tuner
Stereo Decoder
Main Analog
54
PIP Tuner/IF
PIP Comp. Vid.
Main NTSC Video
66
MPEG/AC-3 Audio Decoder
38
50
MPEG Video Decoding / NTSC Video Upconversion / OSD
SDRAM
EEPROM
EEROM
Input
Input
56
NTSC Video Switching
Main
PIP
58
Comb, PIP, & Chroma Decoder
Data Slicer for CC and EDS
TV Ctrl
HSVS
"2H" Video Processing
CRT/Defl. Drivers
To CRT
To Defl. Yokes
52
Convergence OSD
Sandcastle Beam
Serial Async I/P Comm
TV uP
TV chassis
TV Ctrl
EEROM
Power Supply/ Deflection /
LNB Pwr
Pol Ctrl
PFail

Fig. 2

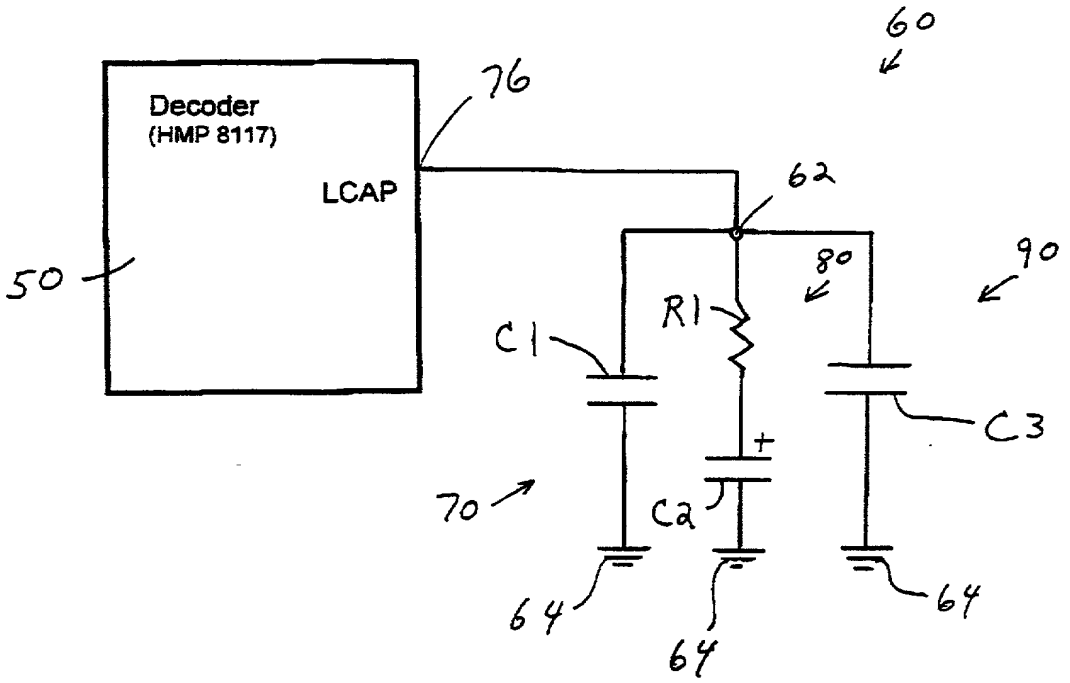

Fig. 3

EXPRESS EL902321714US

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

☐ Declaration Submitted With Initial Filing **OR** ☐ Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	RCA 89413
First Named Inventor	Gerald Adolph Colman etal
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SPURIOUS FREQUENCIES ATTENUATION FOR A DC REFERENCE VOLTAGE

the specification of which *(Title of the Invention)*

☐ is attached hereto

OR

☒ was filed on (MM/DD/YYYY) July 14, 2000 as United States Application Number or PCT International Application Number PCT/US00/19257 and was amended on (MM/DD/YYYY) August 6, 2001 (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56, including for continuation-in-part applications, material information which became available between the filing date of the prior application and the national or PCT international filing date of the continuation-in-part application.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY) Country	Priority Not Claimed	Certified Copy Attached? YES	NO
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐
			☐	☐	☐

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

ApplicationNumber(s)	Filing Date (MM/DD/YYYY)	
US 60/144,426	July 16, 1999	☐ Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

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DECLARATION — Utility or Design Patent Application

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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☐ **Additional inventors are being named on the** _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.